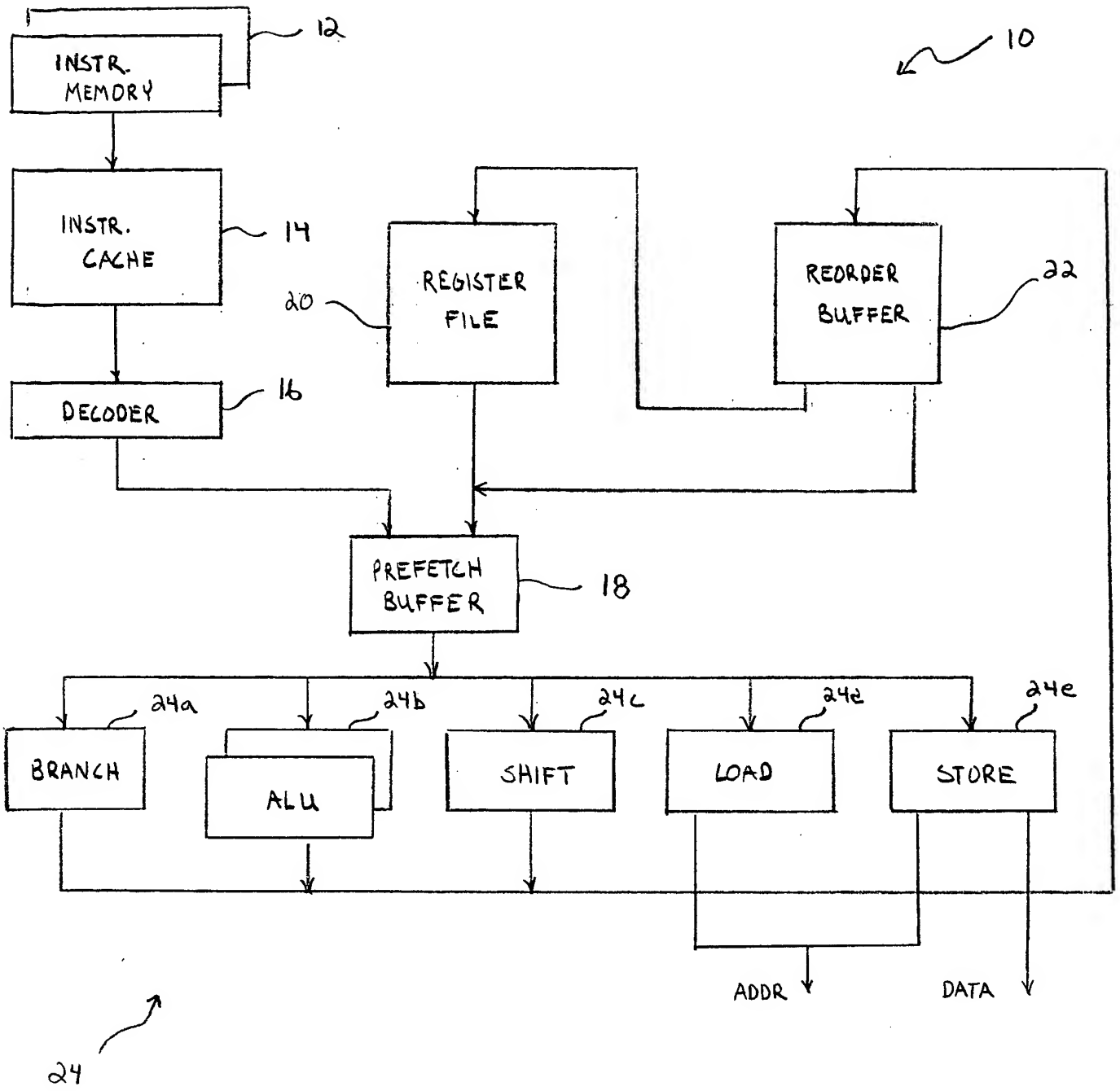
INSTR. MEMORY
12
10
INSTR. CACHE
14
REGISTER FILE
20
REORDER BUFFER
22
DECODER
16
PREFETCH BUFFER
18
24a
24b
24c
24d
24e
BRANCH
ALU
SHIFT
LOAD
STORE
ADDR
DATA
24

FIG. 1

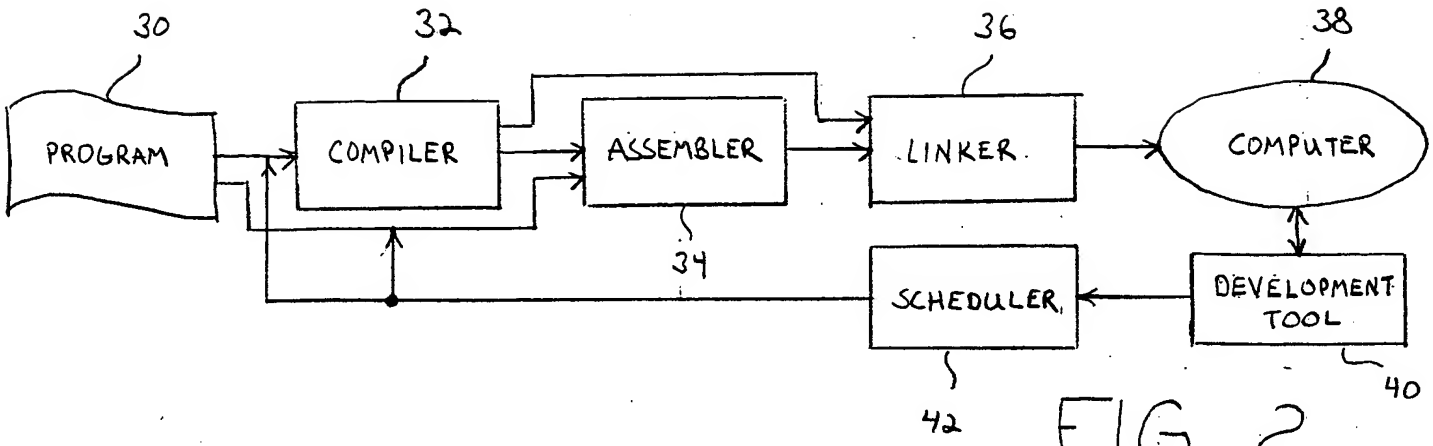

FIG. 2

```
*bp = (*bp & rm[offset]) | ((cd<<offset) & mask)        <- 50

1:  const    tmp1,mask          ;load mask
2:  consth   tmp1,mask
3:  sll      tmp2,cd,offset     ;cd<<offset
4:  and      tmp2,tmp1,tmp2     ;(cd<<offset) & mask
5:  const    tmp1,_rm           ;base address rm
6:  consth   tmp1,_rm                                   } 52
7:  add      tmp1,tmp1,offset   ;address of rm[offset]
8:  load     tmp1,(tmp1)        ;rm[offset]
9:  load     bp,(&bp)           ;*bp
10: and      tmp1,bp,tmp1       ;*bp & rm[offset]
11: or       tmp1,tmp1,tmp2     ;final expression
12: store    tmp1,(&bp)         ;assign *bp
```

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Decode				Execute					Writeback		
I0	I1	I2	I3	ALU1	ALU2	SHF	LS	BRN	R1	R2	Cycle
1:const	2:consth	3:sll	4:and								1
5:const	6:consth	7:add	8:load	1:const		3:sll					2
9:load	10:and	11:or	12:store		2:consth				1	3	3
				4:and	5:const				2		4
				6:consth					4	5	5
					7:add				6		6
							8:load		7		7
							9:load				8
									8		9
				10:and					9		10
					11:or				10		11
							12:store		11		12

FIG. 3

Stage	Issue 1	Issue 2	Issue 3	Issue 4
Write Back	none	none	none	none
Execute	0x1000	0x1001	0x1002	0x1003
Memory 1	0x1006	0x1007	0x1008	none
Memory 0	0x100A	none	none	none
Address Generation	0x100B	0x100D	0x100F	0x1011
Read Data	none	none	none	none
Grouping	0x1013	0x1014	0x1015	0x1016
Fetch/Decode	0x1017	0x1018	0x1019	none

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FIG 4

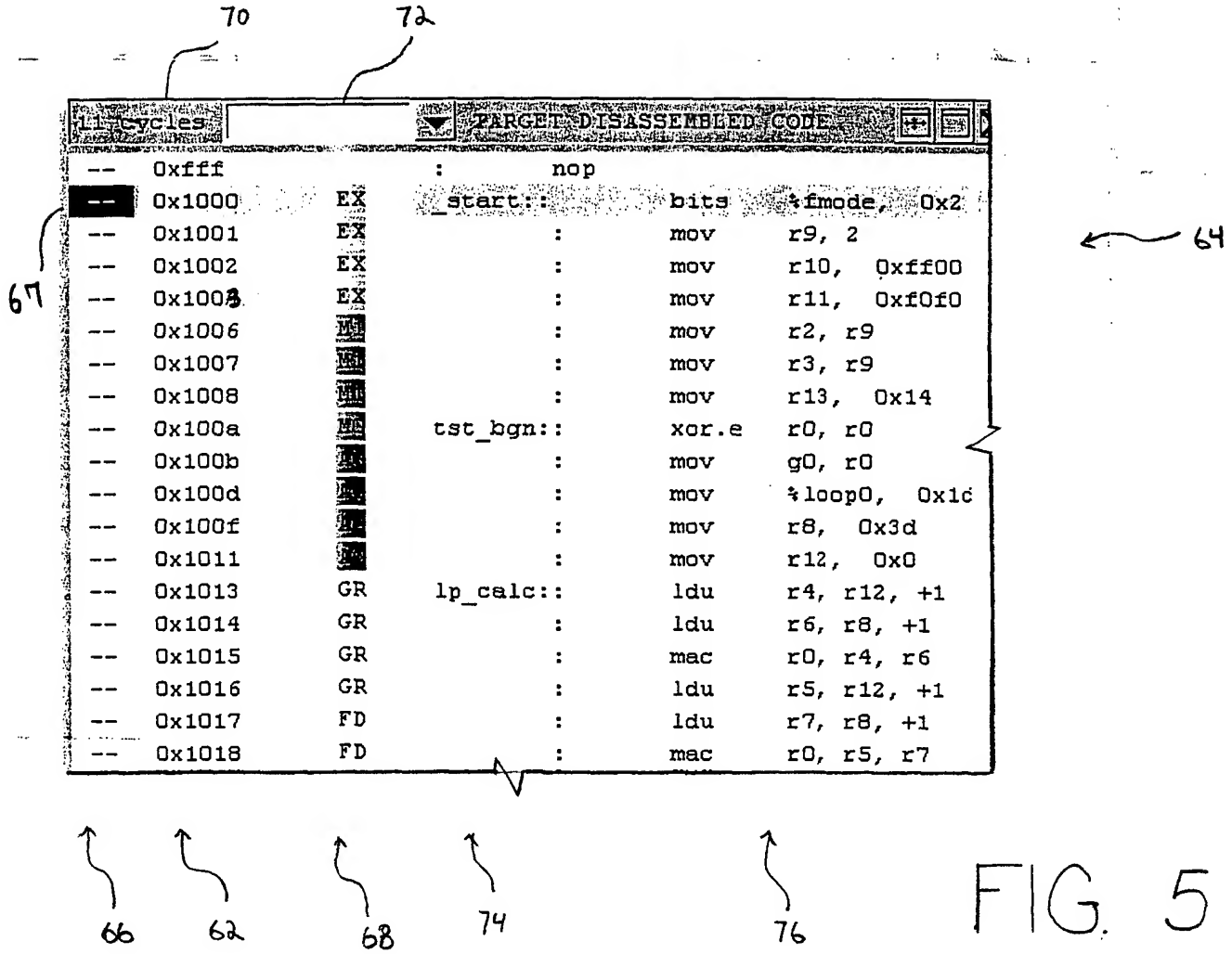

FIG. 5

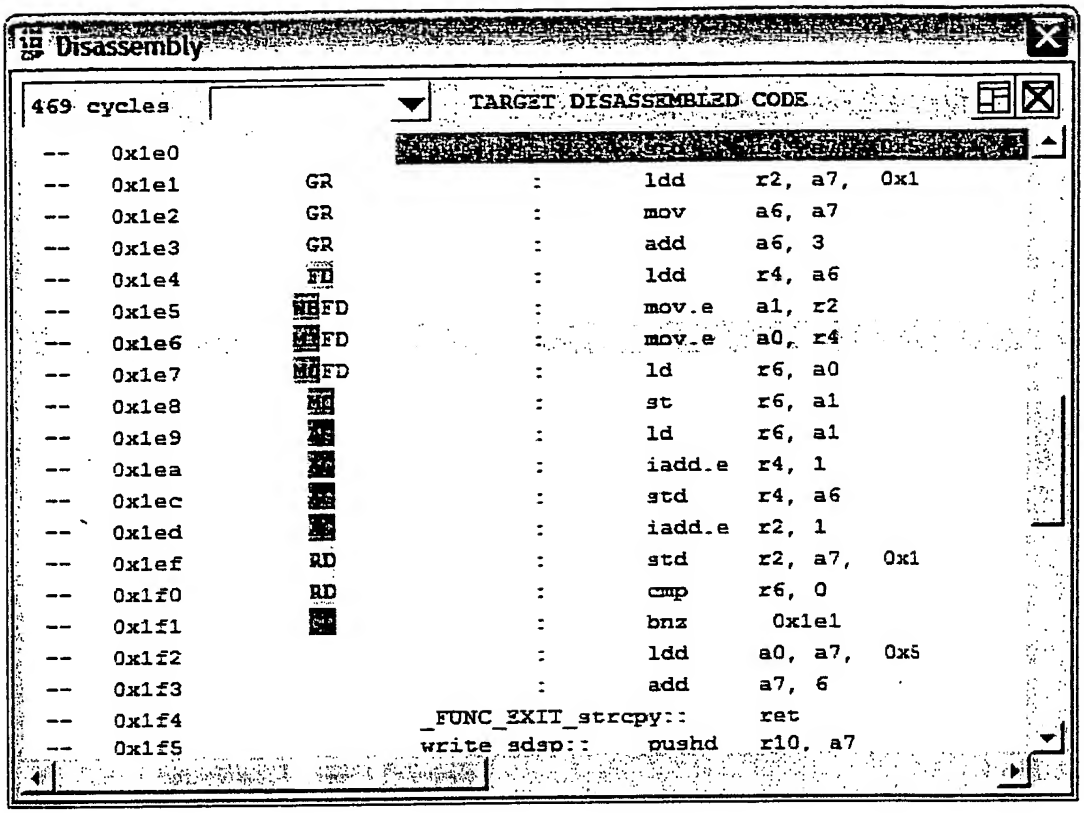

FIG. 6

	FD	GR	RD	AG	MO	M1	EX	WB
T_N	17-19	13-16		b,d f, 11	a	6-8	ϕ-3	
T_{N+1}	17-19	13-16			b,d, f, 11	a	6-8	ϕ-3

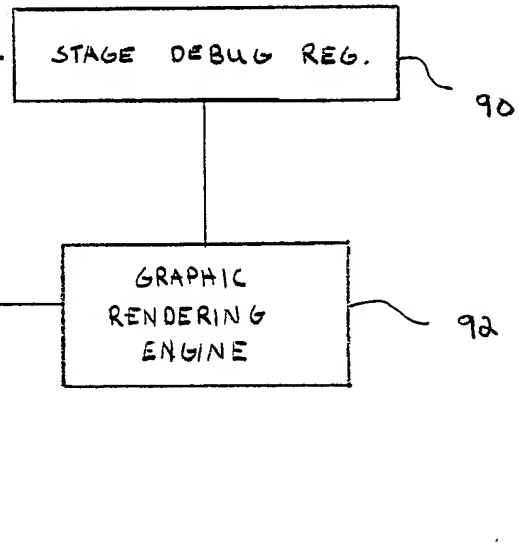

FIG. 7